NTA7002N

Small Signal MOSFET

30 V, 154 mA, Single, N−Channel, Gate ESD Protection, SC−75

ON Semiconductor®

http://onsemi.com

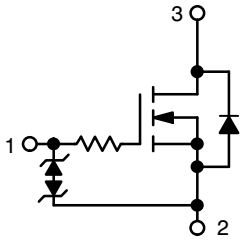
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ @ V_{GS}	I_D MAX (Note 1)
30 V	1.4 Ω @ 4.5 V	154 mA
	2.3 Ω @ 2.5 V	

Features

- Low Gate Charge for Fast Switching
- Small 1.6 x 1.6 mm Footprint
- ESD Protected Gate
- Pb−Free Package is Available

Applications

- Power Management Load Switch
- Level Shift
- Portable Applications such as Cell Phones, Media Players, Digital Cameras, PDA's, Video Games, Hand−Held Computers, etc.



N−Channel

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	30	V
Gate−to−Source Voltage		V_{GS}	±10	V
Continuous Drain Current (Note 1)	Steady State = 25°C	I_D	154	mA
Power Dissipation (Note 1)	Steady State = 25°C	P_D	300	mW
Pulsed Drain Current	$t_P \le 10$ μs	I_{DM}	618	mA
Operating Junction and Storage Temperature		T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)		I_{SD}	154	mA
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

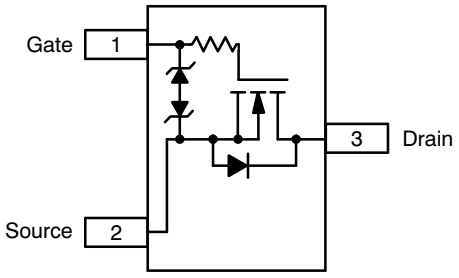
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	416	°C/W

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

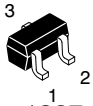
PIN CONNECTIONS

SC−75 (3−Leads)

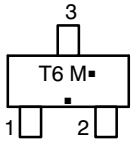


(Top View)

MARKING DIAGRAM



SC−75 / SOT−416
CASE 463
STYLE 5



T6 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTA7002NT1	SC−75	3000 Tape & Reel
NTA7002NT1G	SC−75 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V			1.0	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V, T = 85 °C			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V			±25	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V			±1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V T = 85 °C			±1.0	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 100 μA	0.5	1.0	1.5	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 154 mA		1.4	7.0	Ω
		V_{GS} = 2.5 V, I_D = 154 mA		2.3	7.5	
Forward Transconductance	g_{FS}	V_{DS} = 3 V, I_D = 154 mA		80		mS
CAPACITANCES						
Input Capacitance	C_{ISS}	V_{DS} = 5.0 V, f = 1 MHz, V_{GS} = 0 V		11.5	20	pF
Output Capacitance	C_{OSS}			10	15	
Reverse Transfer Capacitance	C_{RSS}			3.5	6.0	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 5.0 V, I_D = 75 mA, R_G = 10 Ω		13		ns
Rise Time	t_r			15		ns
Turn−Off Delay Time	$t_{d(OFF)}$			98		
Fall Time	t_f			60		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 154 mA		0.77	0.9	V

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

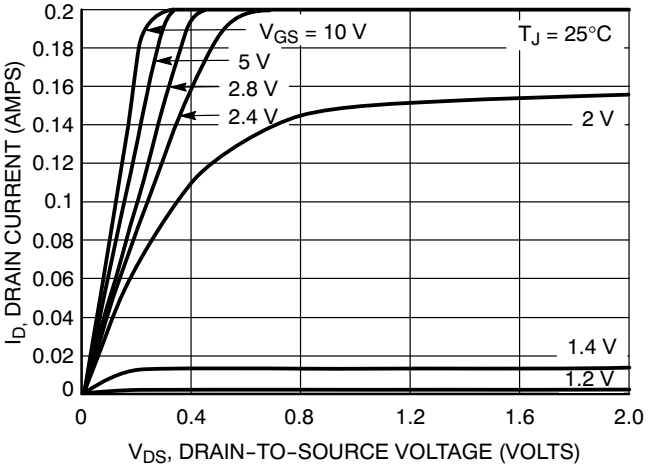


Figure 1. On−Region Characteristics

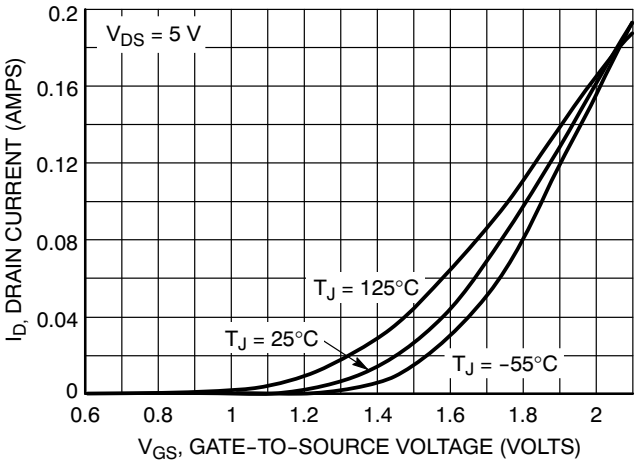


Figure 2. Transfer Characteristics

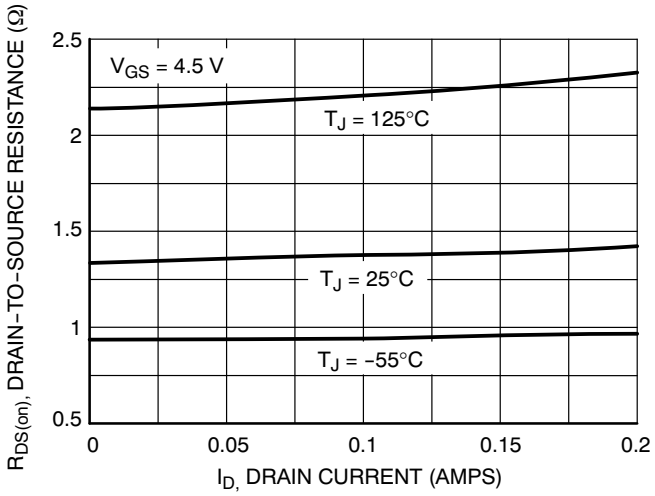


Figure 3. On−Resistance vs. Drain Current and Temperature

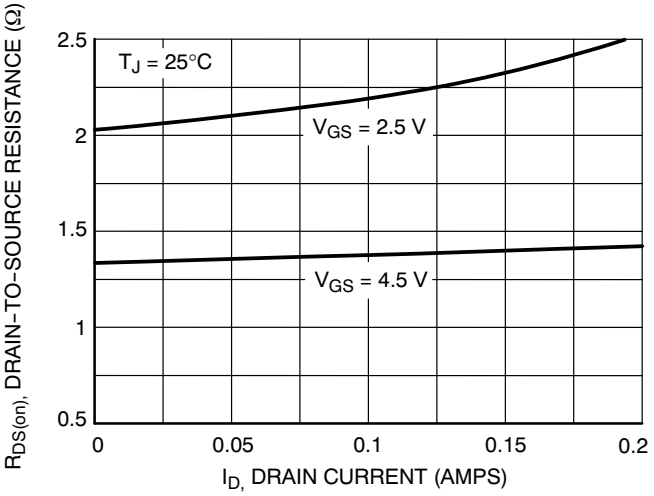


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

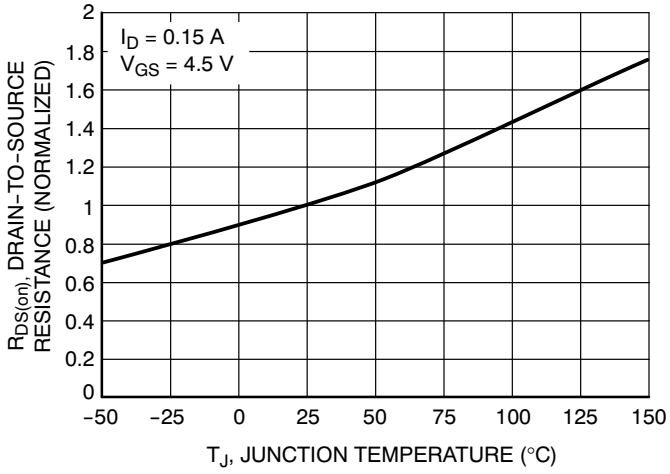


Figure 5. On−Resistance Variation with Temperature

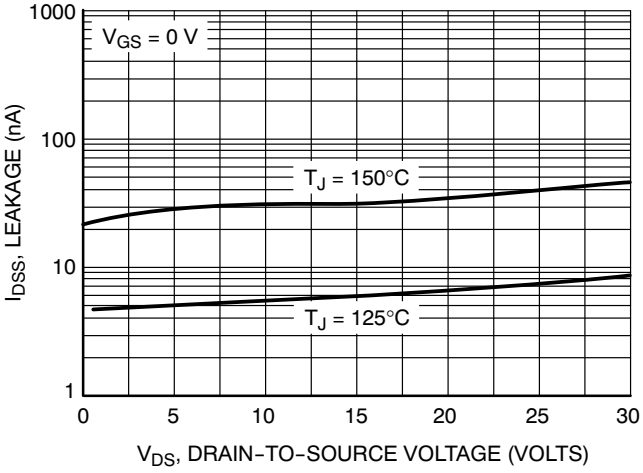


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

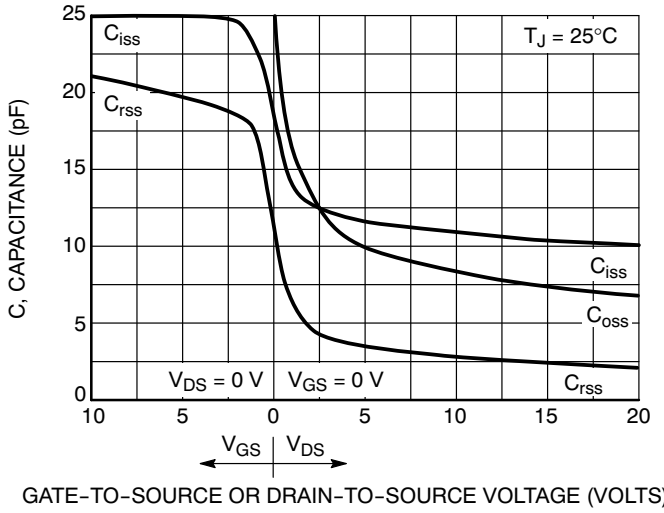


Figure 7. Capacitance Variation

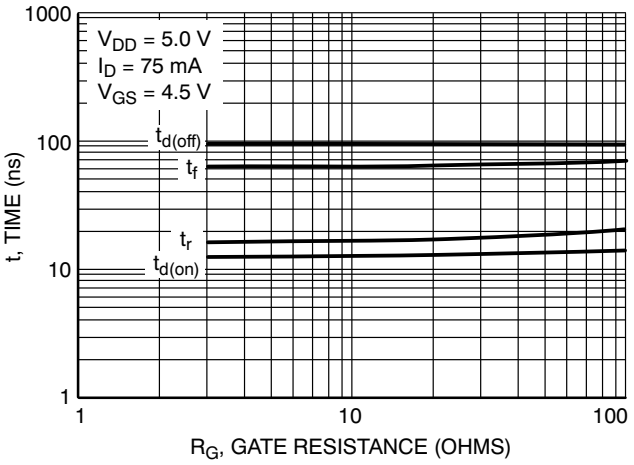


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

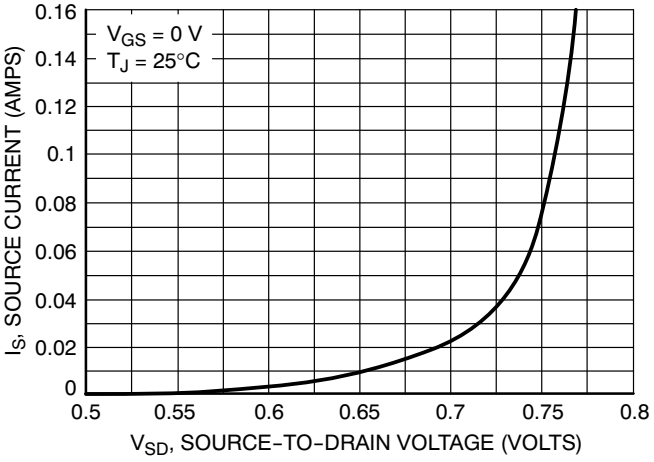
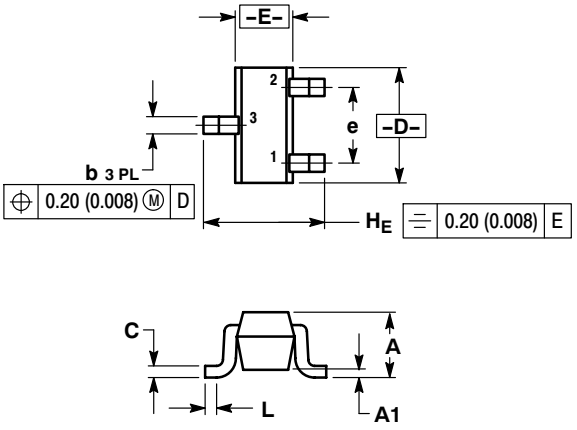


Figure 9. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

SC−75 / SOT−416
CASE 463−01
ISSUE F

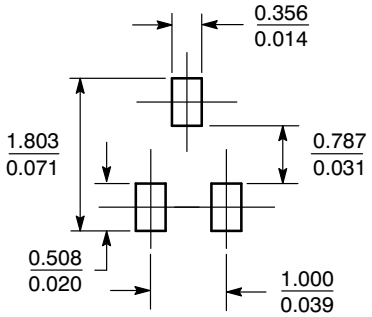


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.059	0.063	0.067
E	0.70	0.80	0.90	0.027	0.031	0.035
e	1.00 BSC			0.04 BSC		
L	0.10	0.15	0.20	0.004	0.006	0.008
H_E	1.50	1.60	1.70	0.061	0.063	0.065

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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